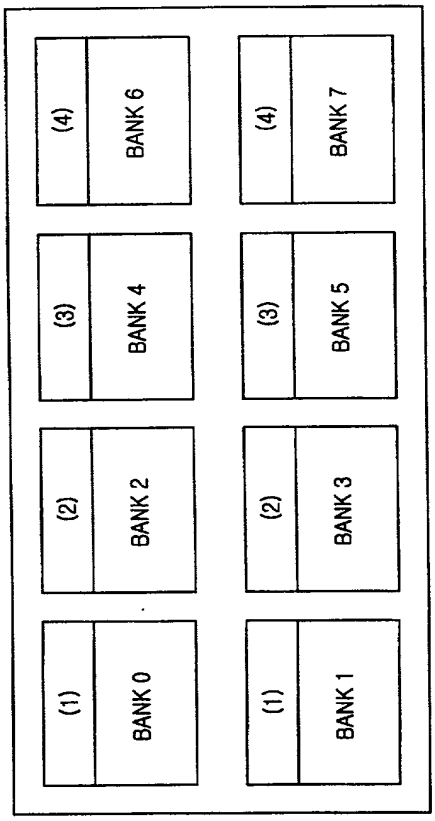

FIG. 1
(PRIOR ART)

FIG. 2

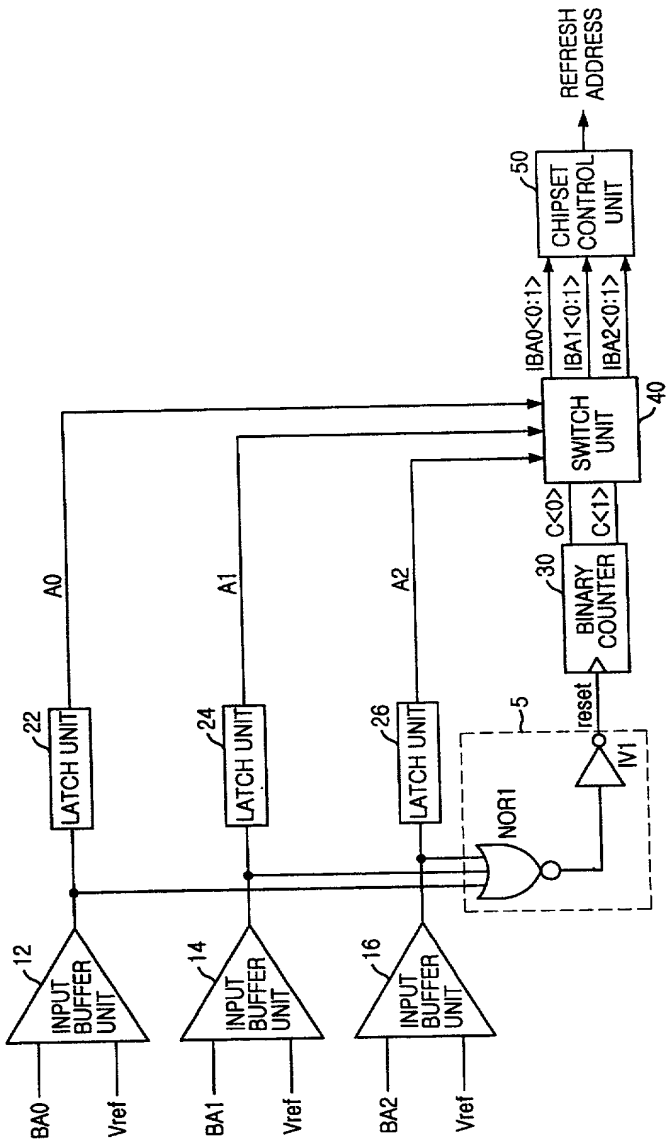
REFRESH ADDRESS
50
CHIPSET CONTROL UNIT
IBA0<0:1>
IBA1<0:1>
IBA2<0:1>
40
SWITCH UNIT
C<0>
C<1>
30
BINARY COUNTER
Ireset
5
IV1
NOR1
A0
A1
A2
22
LATCH UNIT
24
LATCH UNIT
26
LATCH UNIT
12
INPUT BUFFER UNIT
14
INPUT BUFFER UNIT
16
INPUT BUFFER UNIT
BA0
Vref
BA1
Vref
BA2
Vref

FIG. 3

REFRESH COMMAND SIGNAL	BANK COMBINATION CASE 1				BANK COMBINATION CASE 2				BANK COMBINATION CASE 3			
	BA2	BA1	BA0	REFRESH -ING BANK	BA2	BA1	BA0	REFRESH -ING BANK	BA2	BA1	BA0	REFRESH -ING BANK
AUTOMATIC REFRESH	0	0	1	0, 1	0	1	0	0, 2	1	0	0	0, 4
	0	0	0		0	0	X		X	0	0	
AUTOMATIC REFRESH	0	0	0	2, 3	0	0	1	1, 3	0	0	0	1, 5
	0	1	X		0	X	1		X	0	1	
AUTOMATIC REFRESH	0	0	0	4, 5	0	0	0	4, 6	0	0	0	2, 6
	1	0	X		1	X	0		X	1	0	
AUTOMATIC REFRESH	0	0	0	6, 7	0	0	0	5, 7	0	0	0	3, 7
	1	1	X		1	X	1		X	1	1	